Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] *1.*An amplifying method of a clock signal of an liquid crystal display (LCD) driving circuit, for amplifying a periodic clock signal swinging between a first original level and a second original level to a target signal swinging between a first target level and a second target level, wherein the first original level is higher than the second original level, the first target level is higher than the second target level, the first target level is higher than the first original level, and the second target level is lower than the second original level, the amplifying method for a clock signal of an LCD driving circuit comprising:
amplifying the clock signal to a relay signal that swings between a first relay level and a second relay level, wherein the first relay level is higher than the second relay level; and
amplifying the relay signal to the target signal,
wherein the first relay level is between the first original level and the first target level, the second relay level is between the second original level and the second target level.

[c2] *2.*The amplifying method as recited in claim *1*, further

comprising receiving the clock signal in a predetermined period.

[c3] *3.*A driving stage for an LCD driving circuit, the driving stage being part of the LCD driving circuit in a cascade fashion, the driving stage comprising:
a clock input terminal, for receiving a clock signal having one of a first original level and a second original level;
a level shifter, coupling to the clock input terminal, for receiving the clock signal from the clock input terminal, operating at a first target level and a second target level, for amplifying the clock signal to a relay signal having a first relay level and a second relay level; and
an output buffer, coupling to the level shifter, for receiving the relay signal from the level shifter, operating at the first target level and the second target level, for amplifying the relay signal having one of the first target level and the second target level,
wherein the first original level is higher than the second original level, the first target level is higher than the second target level, the first relay level is between the first original level and the first target level, and the second relay level is between the second original level and the second target level.

[c4] *4.*The driving stage as recited in claim *3*, wherein the output buffer comprises an odd number of inverters.

[c5] *5.*The driving stage as recited in claim *3*, wherein the output buffer is made of complementary metal-oxide-semiconductor (CMOS) inverter.

[c6] *6.*The driving stage as recited in claim *3*, wherein the level shifter comprises a plurality of inverters that are made of n-type thin film transistor and p-type thin film transistor.

[c7] *7.*The driving stage as recited in claim *6*, wherein the inverters of the level shifter have a thin film transistor that is self-connected drain/source and gate.

[c8] *8.*The driving stage as recited in claim *3* further comprising a dynamic register, wherein the dynamic register couples the clock input terminal to the level shifter, and determines whether to conduct the clock input terminal to the level shifter according to a control signal module.

[c9] *9.*The driving stage as recited in claim *8*, wherein the dynamic register comprises:
a register output terminal, coupling to the level shifter;
a first control signal input circuit, receiving a previous stage driving signal from a previous driving stage, and determines whether to conduct the clock input terminal to the register output terminal according to the previous stage driving signal; and

a second control signal input circuit, receiving a next stage driving signal from a next driving stage, and determines whether to conduct the register output terminal to the second target level according to the next stage driving signal.

[c10] *10.*The driving stage as recited in claim *8*, wherein the dynamic comprises:
a register output terminal, coupling to the level shifter;
a first control signal input circuit, receiving a previous stage driving signal from a previous driving stage, and determines whether to conduct the clock input terminal to the register output terminal according to the previous stage driving signal;
a second control signal input circuit, receiving the previous stage driving signal and output of the level shifter, and determines whether to conduct the driving stage to the second target level thereby.

[c11] *11.*The driving stage as recited in claim *10* further comprising:
a level chopper, couples the first target level to the register output terminal, and determines whether to conduct the register output terminal to the first target level according to the previous stage driving signal.

[c12] *12.*The driving stage as recited in claim *11*, wherein the

level chopper comprises p-type thin film transistor.